A Brief Introduction to the JTAG Boundary Scan Interface

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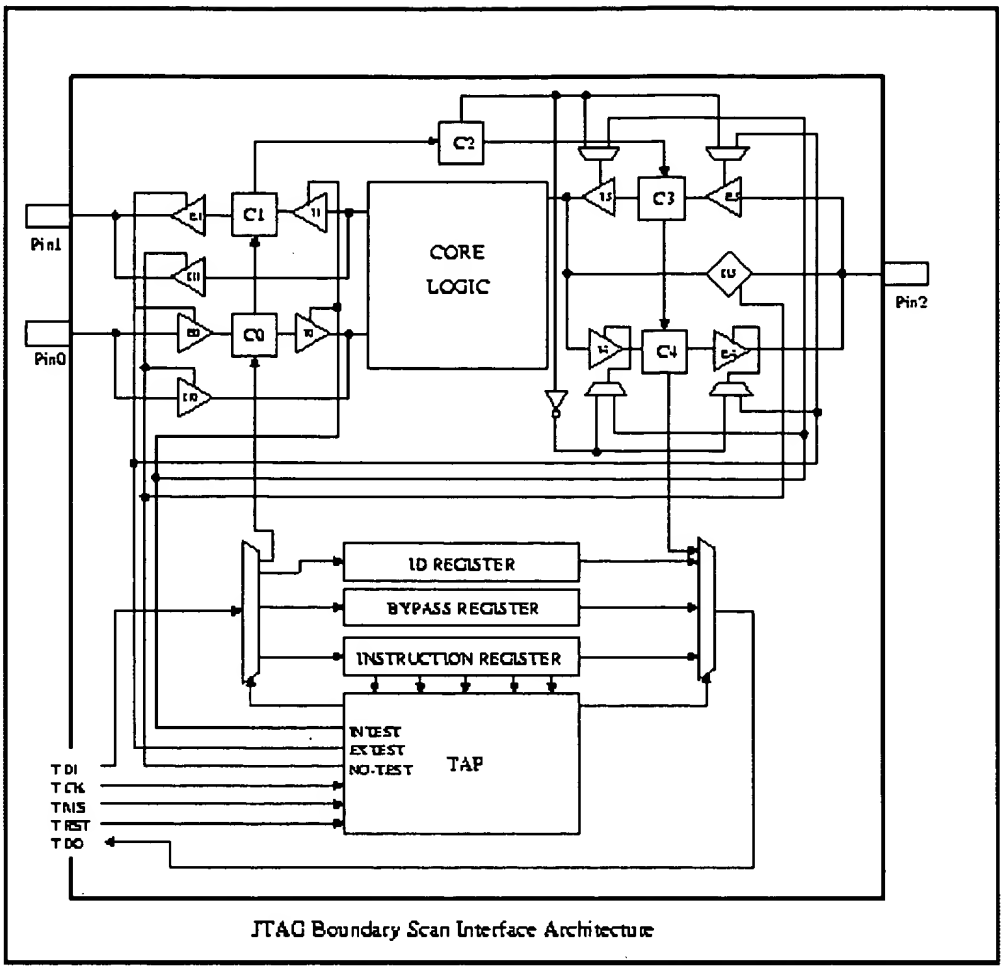
One of the difficult areas in the development of any modern hardware system is the production-testing of the Printed Circuit Boards (PCBs). This is the problem addressed by the IEEE standard number 1149 "Standard Test Access Port and Boundary-Scan Architecture". This standards defines a 5-pin serial protocol for accessing and controlling the signal-levels on the pins of a digital circuit, and has some extensions for testing the internal circuitry on the chip itself (which will not be discussed here). The standard was written by the Joint Test Action Group (JTAG) and the architecture defined by it is known as "JTAG boundary scan" or as "IEEE 1149".

The general structure of the JTAG boundary scan test interface is shown in the following figure.



JTAG Boundary Scan Interface Architecture

All the signals between the chip's core logic and the pins are intercepted by a serial scan path known as the "*Boundary Scan Register*" (*BSR*), and shown as cells "C0", "C1", "C2", "C3", and "C4" in the figure above. In normal system operation this path can transparently connect the core-logic signals to the pins and effectively become invisible. In external-test mode, it can disconnect the core-logic from the pins, drive the output pins ("Pin1", and "Pin2" in the figure above) by itself, and read and latch the states of the input pins (figure: "Pin0", and "Pin2"). In internal-test mode, it can disconnect the core-logic from the pins, drive the core-logic input signals by itself, and read and latch the states of the core-logic output signals.

In the figure above, and assuming that the JTAG interface is in external-test mode, C0 is the BSR cell capturing the state of the input pin 0. C1 is the BSR cell driving the output pin 1. C2 does not itself correspond to any specific pin, but it is the "enable" BSR cell which controls the "direction" of the bidirectional pin 2. C3 is the input BSR cell capturing the state of the bidirectional pin 2, and C4 is the output BSR cell driving the bidirectional pin 2. Summarizing we can identify three times of BSR cells:

- *Input Cells* like C0, and C3. They are always associated with a specific pin whose state they capture when the JTAG interface is in external test mode.
- *Output Cells* like C1, and C4. They are always associated with a specific pin which they drive when the JTAG interface is in external test mode.
- *Enable Cells* like C2. They are not associated with any pin per-se, but they either control the direction of bidirectional pins, or enable and disable certain input or output pins.

Gates E0, E3, and E4 operate under the control of the TAP (and probably also under the control of